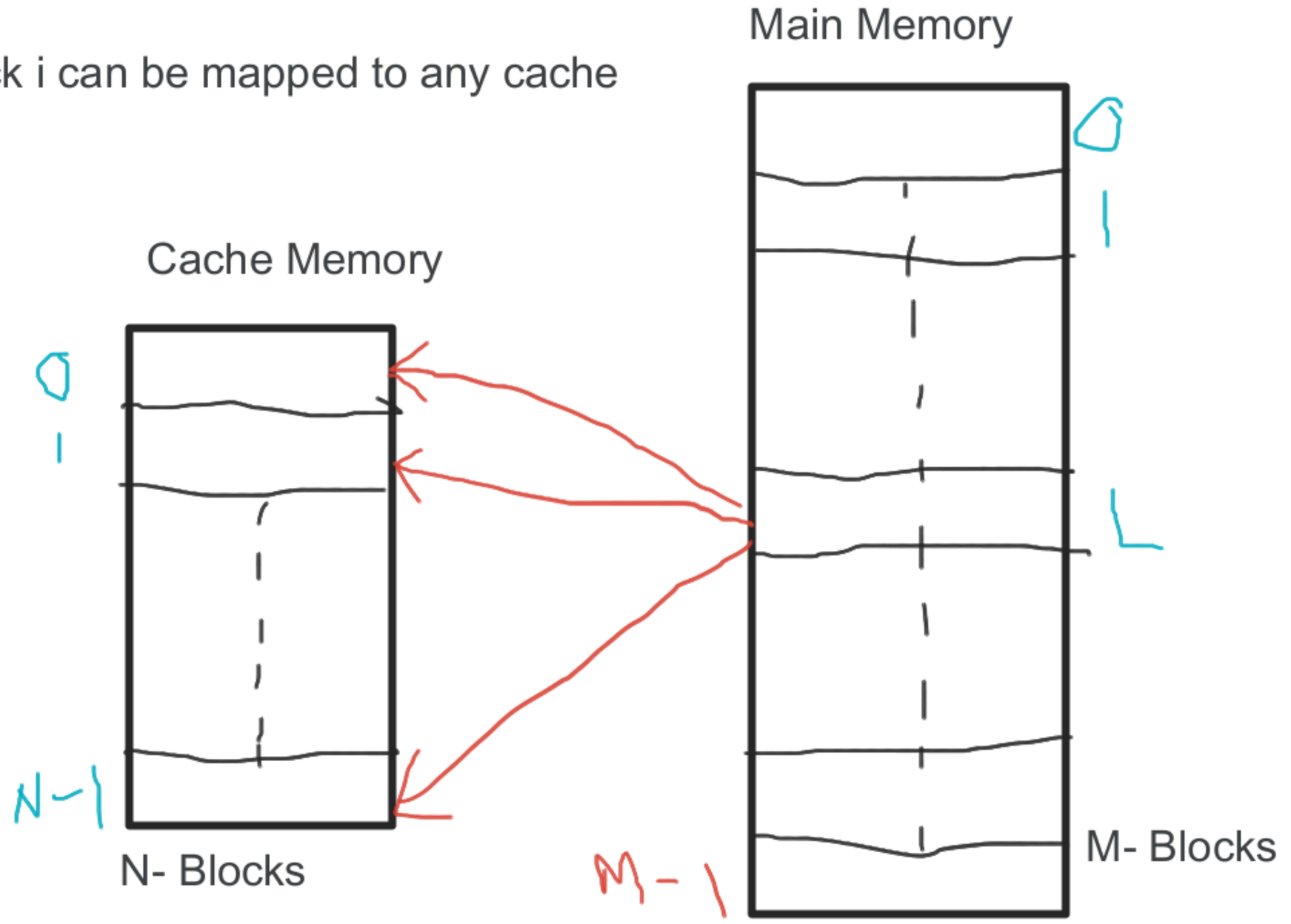
Fully Associative Mappnig

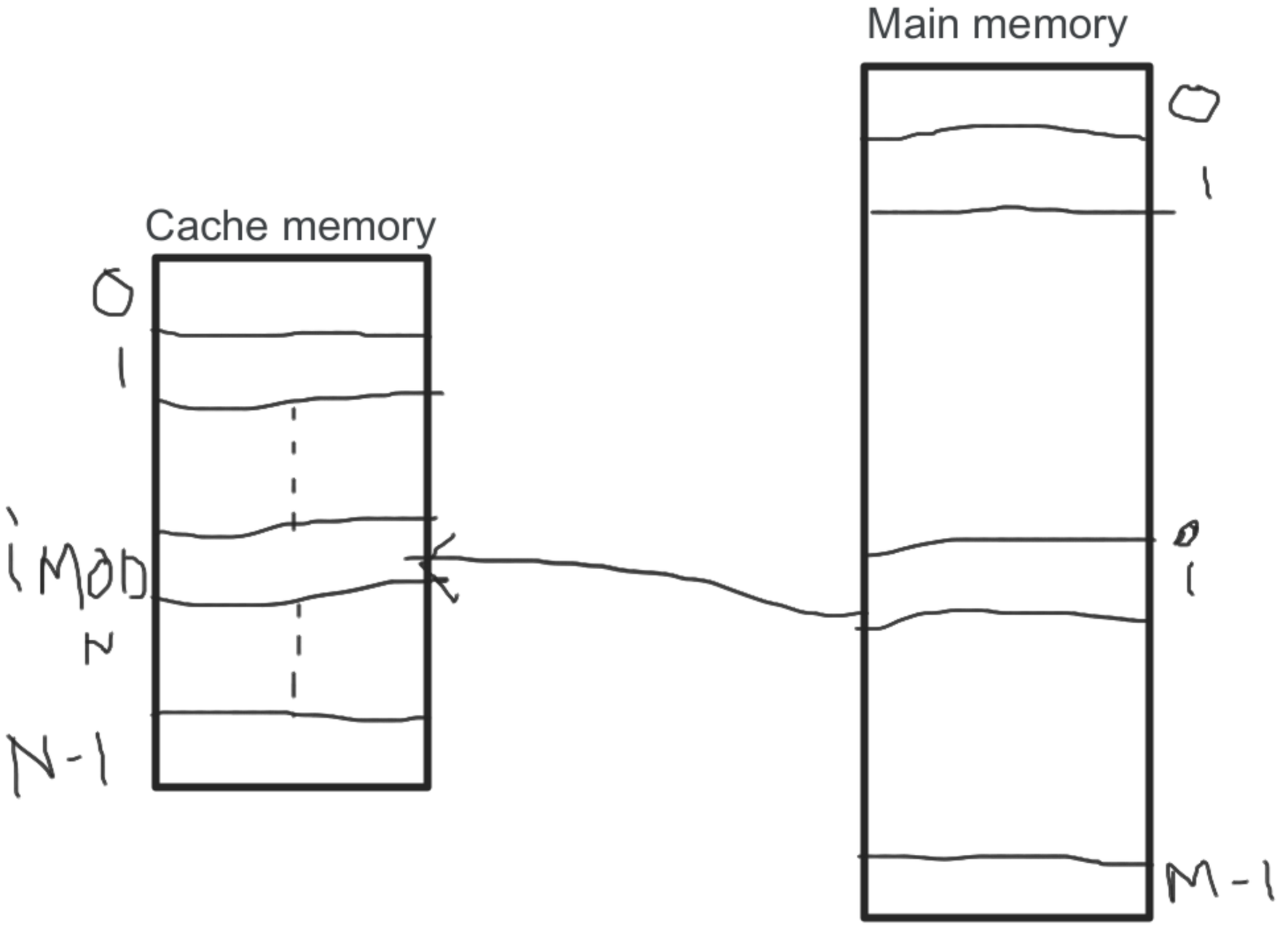
main memorry block i can be mapped to any cache block j

0<= i <= 1
0<= j <= (N-1)

m -bits



Direct Mapping



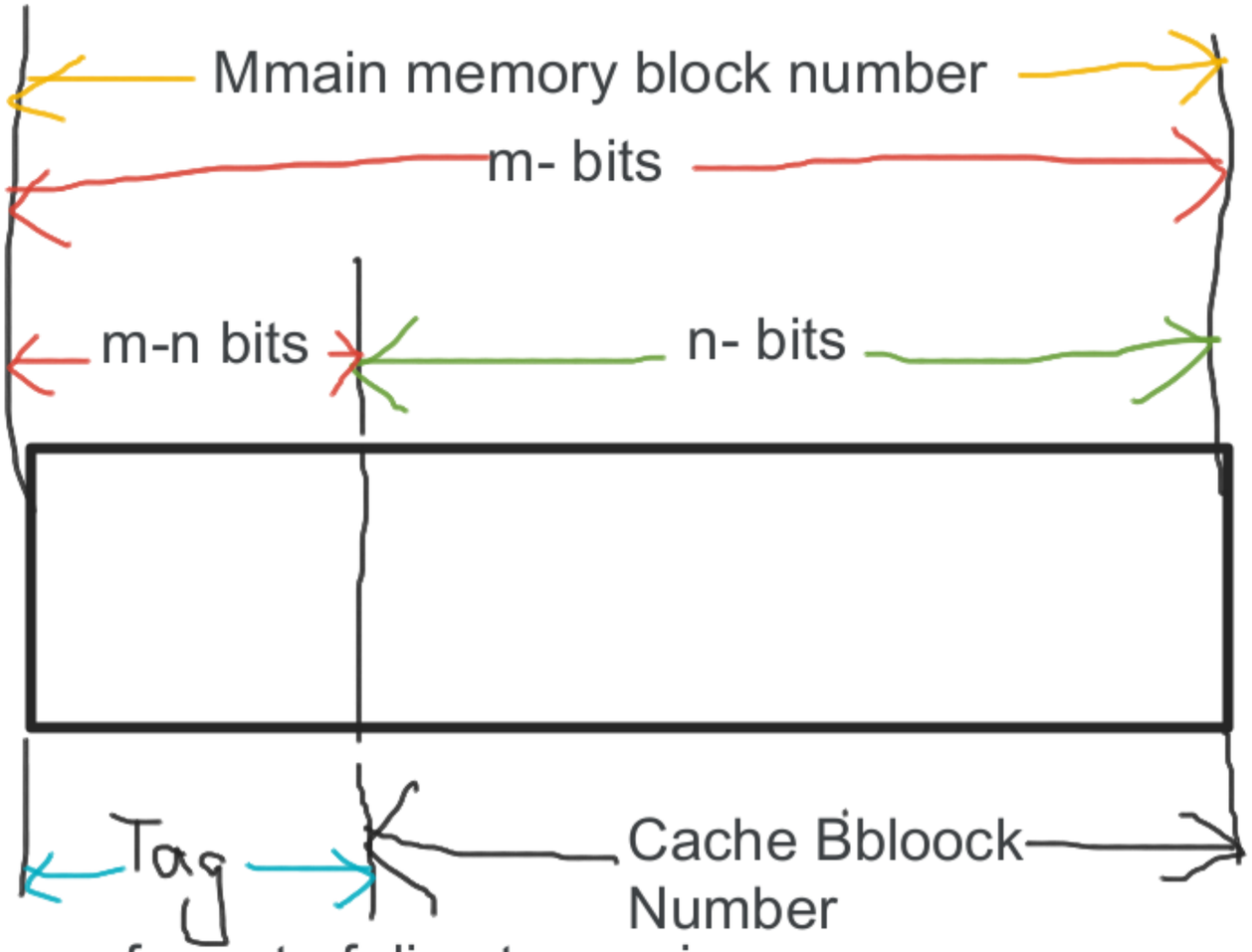
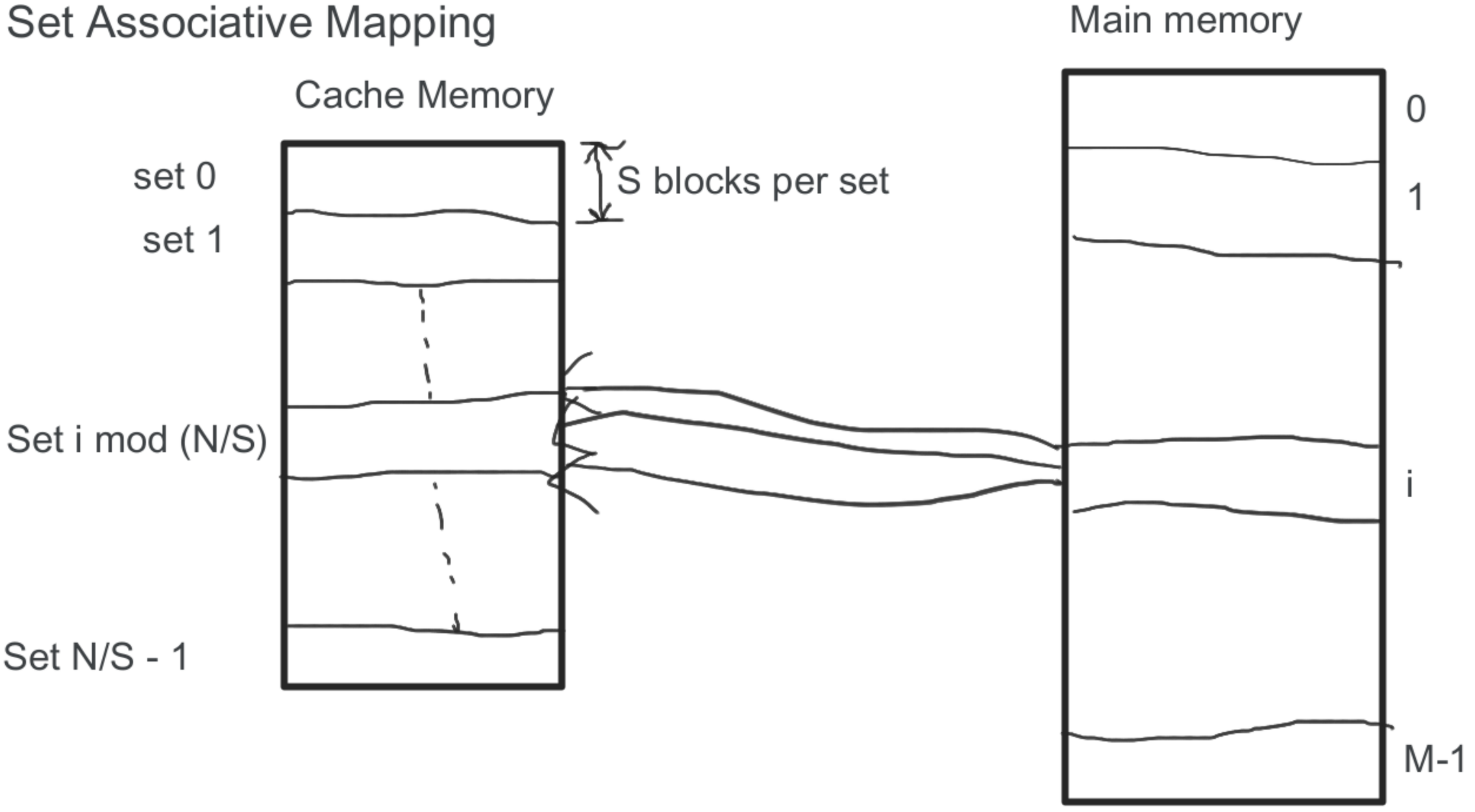


fig name : Address format of direct mapping

Set Associative Mapping



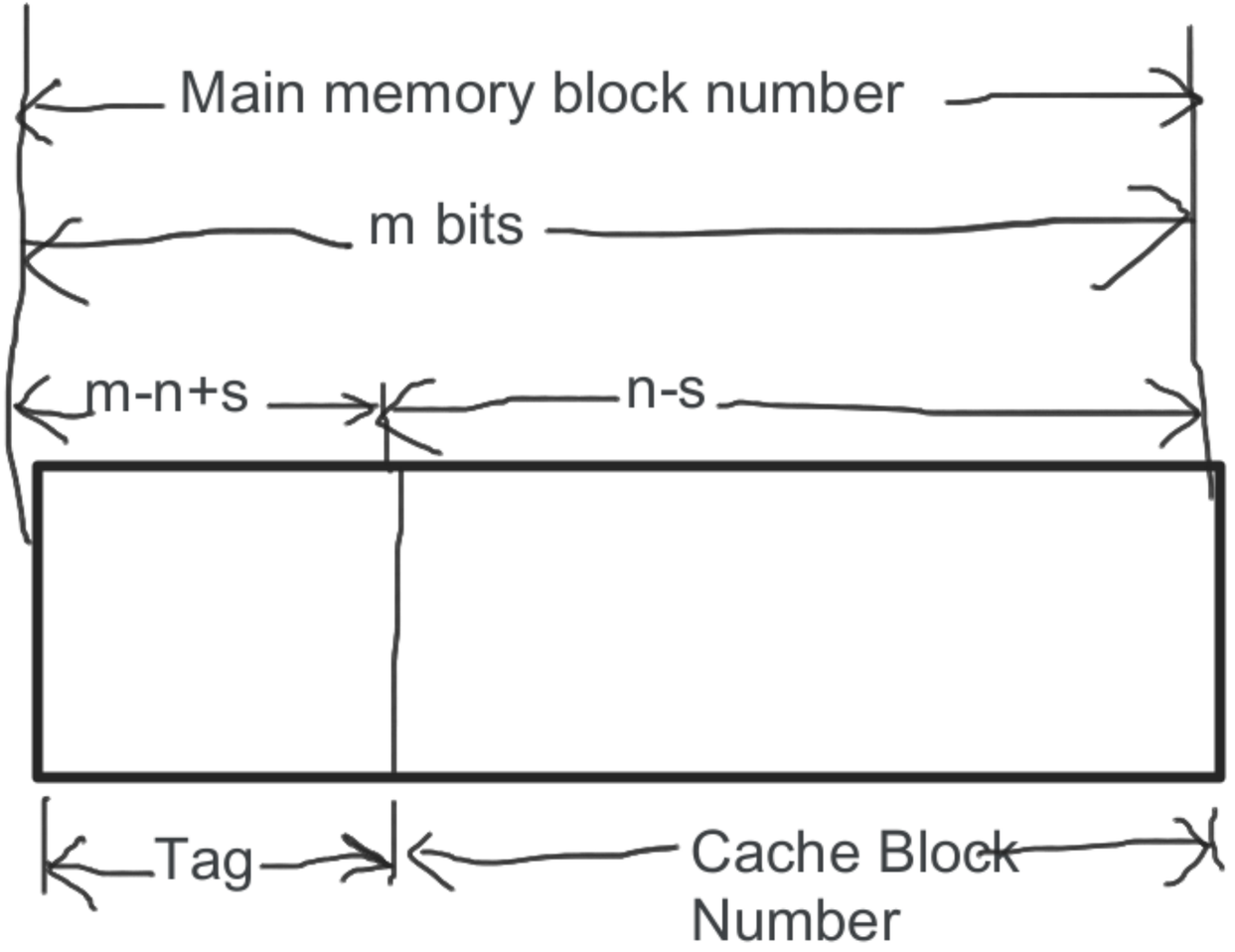


Fig Name : Adress format under set associative mapping

If $M=2^m$ M is total block of main memory

$N= 2^n$

Cache block per Set $S= 2^s$

Range of 0 to N/S - 1

Tag will be m- (n-s)

generic model of an I/O module

Define I/O module

***des. I/O module with Structure diagram

** Draw Intel 82C55 A Programmable peripheral Interface and describe this

Direct memorry Access (DMA) with Diagram

Chapter 7

Input/Output

***8237 DMA system Bus with diagram

*** Describe I/O Channel characteristics with diagram